System Level Low Power Design Issues and Challenges

Tom Quan
TSMC

Outline

- Market/Design Trend
- System-Level Design
- System-Level Low Power Modeling
- Issues and Challenges
- Conclusion

TSMC Property

Where Are the Growth?

	Smartphone	Cloud Data Center	IoT
			
CAGR 12' – 17'	20%	24%	30%

Source: TSMC Estimation; Gartner Research

Low Power Everywhere …

Smartphone

1-2 days

Battery

Week

Cloud Data Center

100B KWh

Cooling

10B KWh

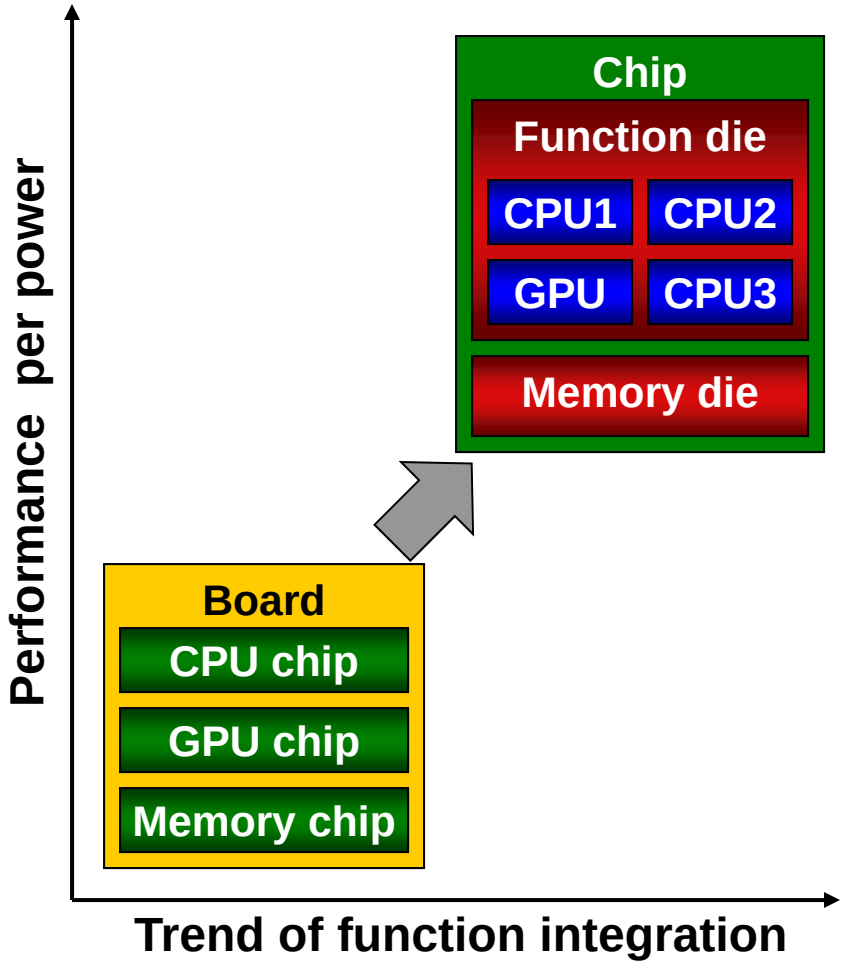
IoT

Week

Battery

Month

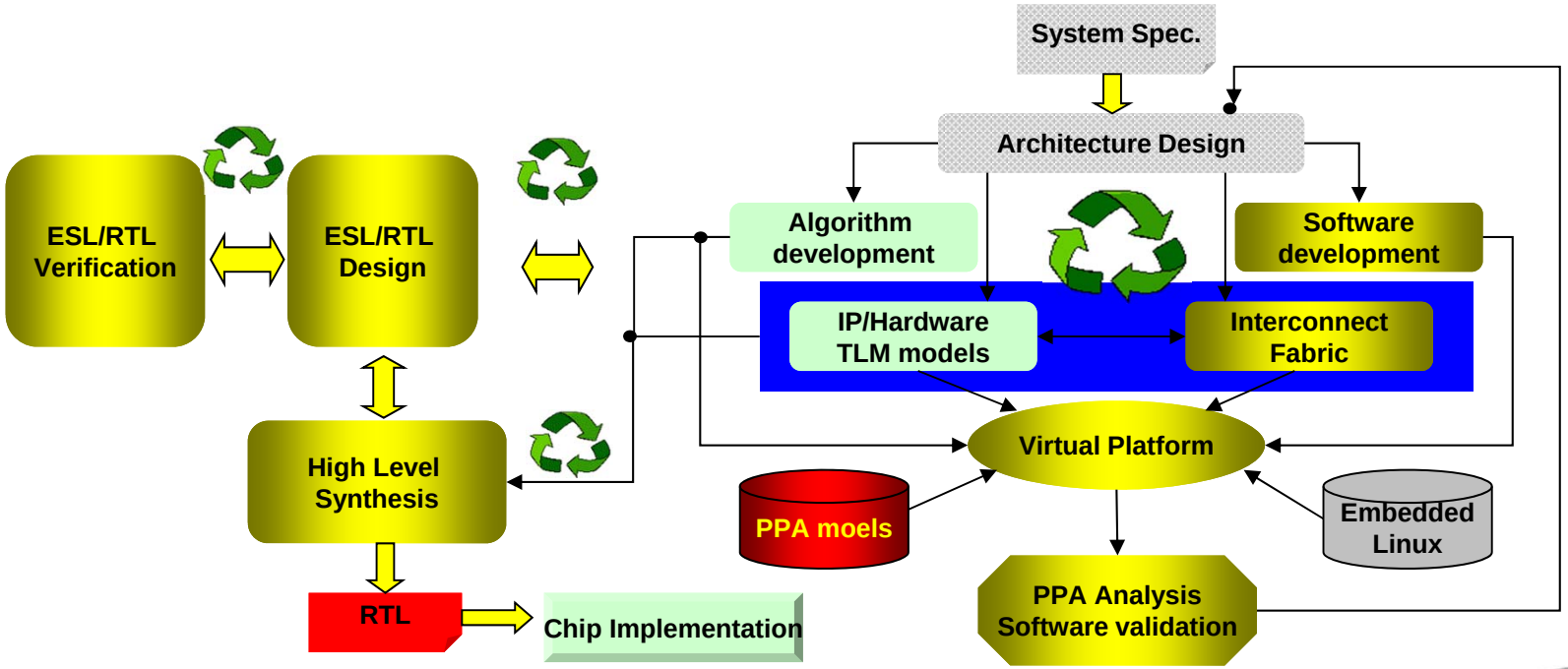
More and More Functions …



- Optimized architecture to reduce power in early stage
  - ESL Design
- High performance application with advance process
  - Multi-core in one die
    - SoC Interconnect Fabric
  - Multi-die in one chip
    - 3DIC with TSV
    - System in Package

System Level Design

- Virtual Platform
- ESL Verification
- High Level Synthesis

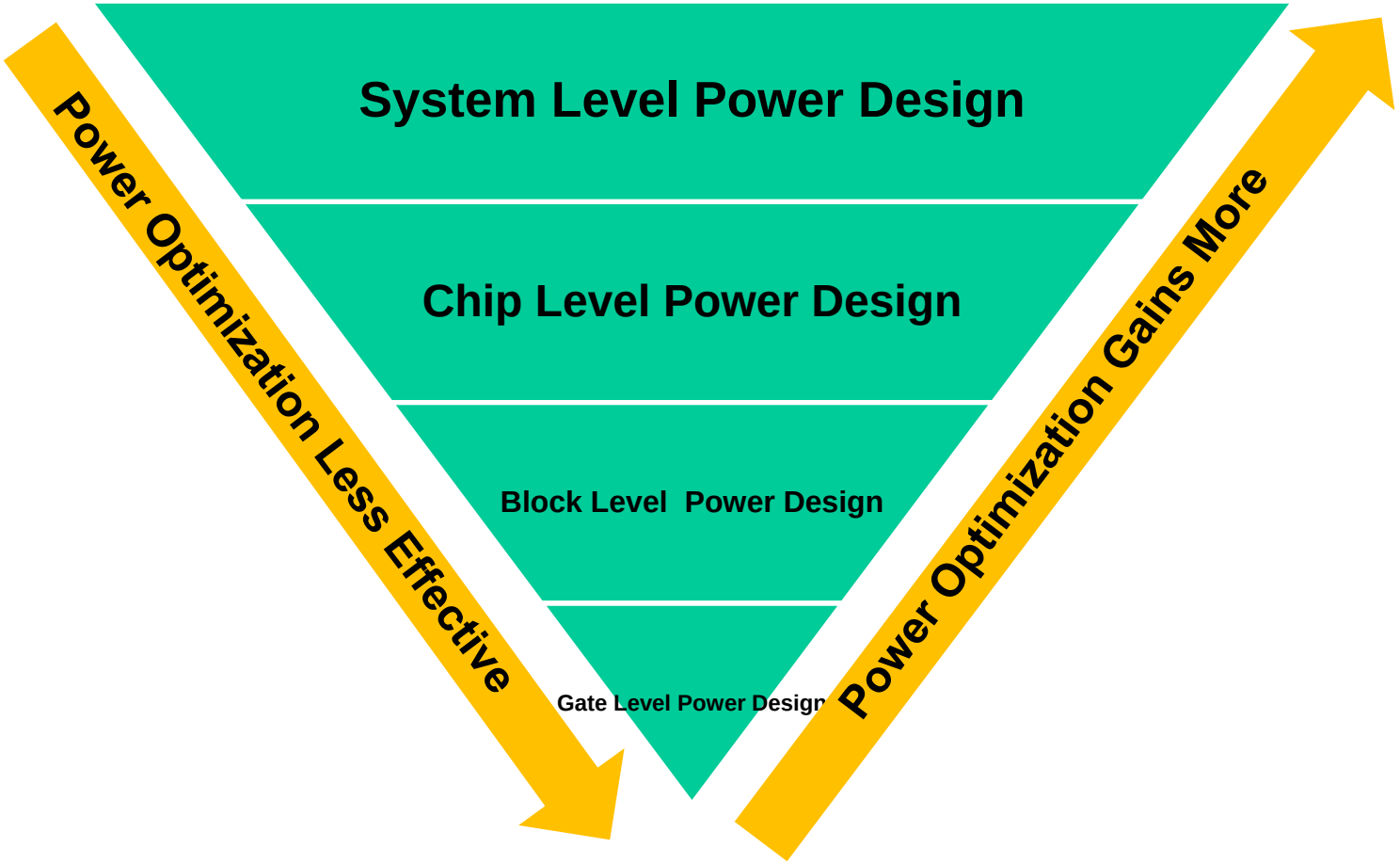


Low Power Design at Every Level

- **System level**
  - **HW/SW tradeoff and partition, CPU choice, cache level and memory subsystem, bus structures, DVFS, etc.**
- **Chip/Block/Gate level**
  - **Power planning, power domain, power gating, clock gating, CTS, leakage power optimization**

Need design teams attention at every level of design abstraction!

Low Power Design Gain/Loss



- System level power optimization gains most savings
- Late stage power optimization misses critical design decisions

Low Power Modeling

- Power modeling key to system level power design
  - Applications and use-case
  - OS level or bare-metal level
- Power models maybe algorithm-based, maybe functional block-based
- Technology ties and dependency make power models more accurate
- Ecosystem partners (EDA, IP and Foundries) collaborations are essential

Issues and Challenges

- What to model, how to model
  - Timing, power and power states
  - Functional behavior
  - Ease of modeling
  - Accuracy vs runtime tradeoff
- Technology dependence and correlation
- Agnostic modeling, methodology and platform for system level low power optimization
- HW/SW partition and co-design: HW saves power for SW, SW works with HW's intention

Conclusion

- System level design enables most power efficient architecture
- System level low power modeling is key to early power optimization
- Collaboration and industry standard needed for the next level
- The earlier, the better and mores savings in power

Thank You !