IEEE P2416 Standard for Power Modeling

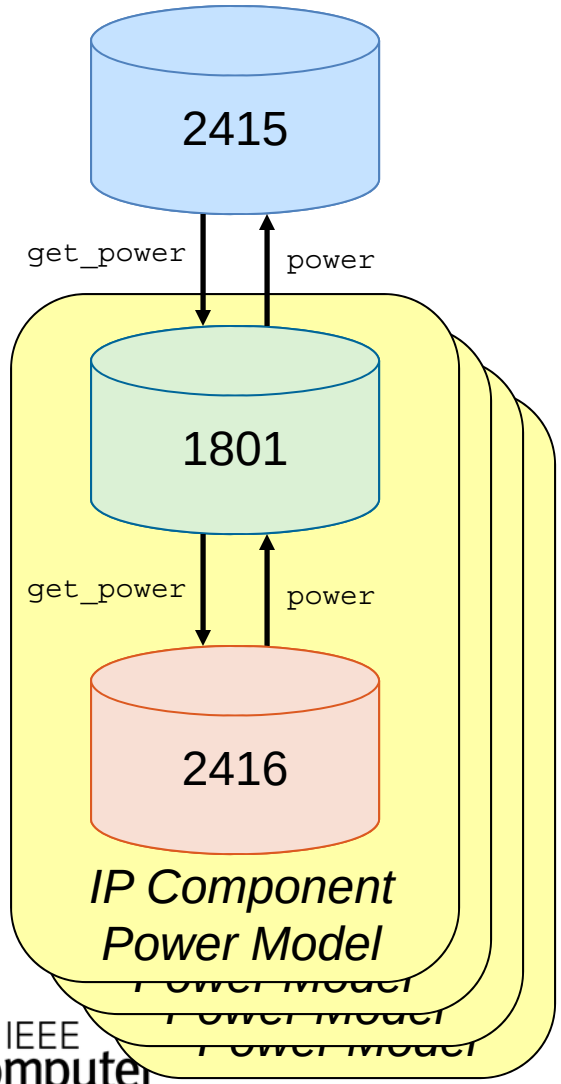
Nagu Dhanwada, Chair, IEEE P2416 WG
Jerry Frenkil, Vice-Chair, IEEE P2416 WG

IEEE computer society

DASC

IEEE

Power Model Data Flow: 1801-2415-2416



- Unified power abstraction of components and the whole device for FW, OS and apps development
- Describes SW/system-level clocks, voltages, states/transitions, events/control, latencies/power
- Connects the power/energy design flow of HW and SW, IP producers and integrators

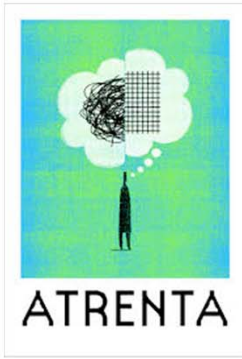
- IP Component Power State Model
- Power domains for the component
- Power state definitions per power domain
- Legal transitions between power states
- Power function for each power state

- IP Component state-based power data
  - Semantics for power/energy views of complex IP
  - Formalized PVT independence
    - Power contributors per (power & functional) mode
    - Energy contributors per mode transition
  - Computationally efficient PVT binding
  - Multi level organization for multiple views

IEEE computer society

IEEE

WHO is involved?



WHAT is the standard trying to address?

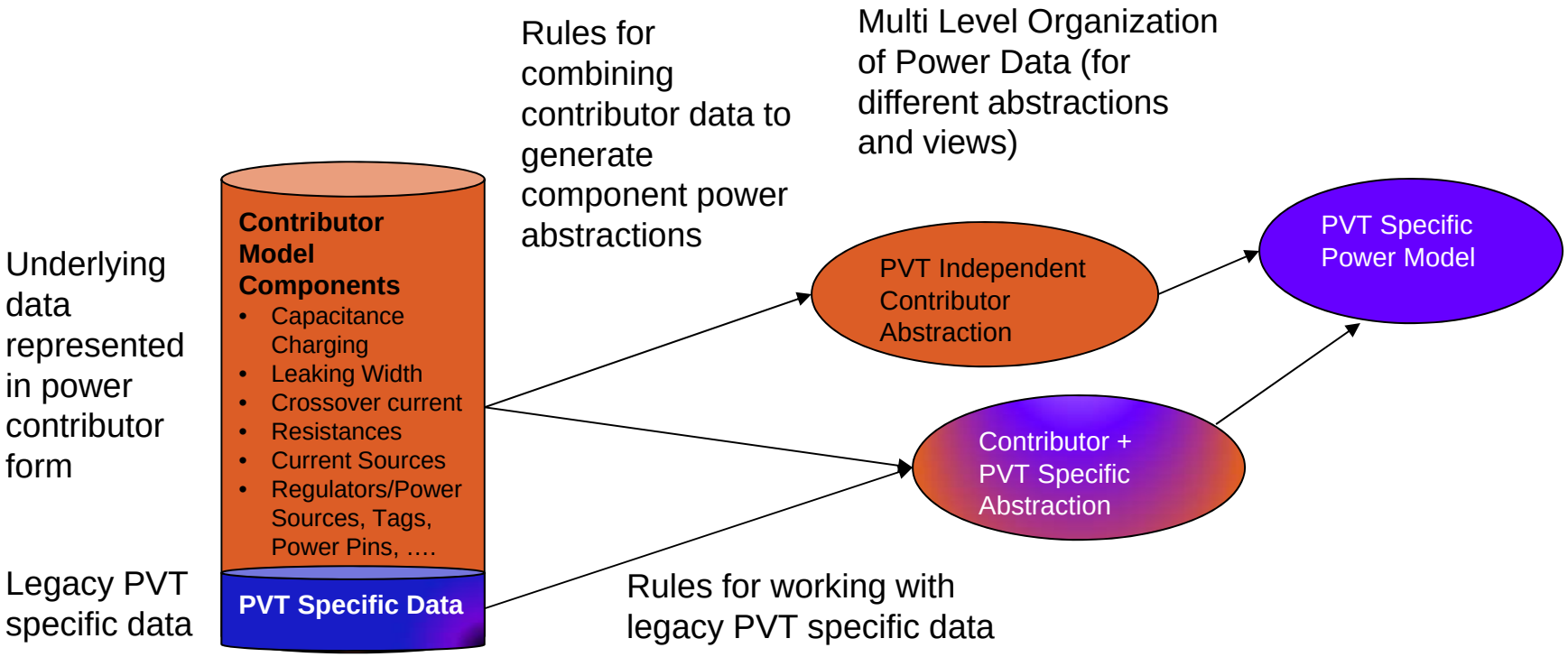
- IP and Component Abstraction
- PVT (Process, Voltage and Temperature) Independent Modeling
- Model Continuity and Inter-operability
  - Within Design Flows
  - Across Abstraction Levels

WHY do we need to address these?

- Power aware system sims need efficient models
  - Abstraction essential for providing major efficiency gains
- Systems are often composed of a diverse set of components
  - Formalism provides a common structure for deriving and representing abstractions
- Per-corner PVT characterization is a significant burden
  - PVT Independent modeling substantially reduces effort for
    - Multi-corner characterization
    - Inaccurate interpolation / extrapolation
- Power model re-use
  - Contributor modeling enables the use of a single power model from early spreadsheet-style modeling to detailed simulations during rest of design flow

HOW will we do it?

Intelligent abstraction and efficient parameterization



For details and results of using this type of flow on a real microprocessor at IBM, please see *Efficient PVT Independent Abstraction of Large IP Blocks for Hierarchical Power Analysis*, Dhanwada, et. al., ICCAD 2013

WHO will benefit?

- Model producers
  - Soft IP providers
  - Hard IP providers & Foundries
  - Architects & Design explorers
- Model consumers
  - Architects & Design explorers
  - SoC integrators
  - EDA developers

Want to Join Us?

Please contact

Nagu Dhanwada nagu@us.ibm.com

Jerry Frenkil jfrenkil@si2.org