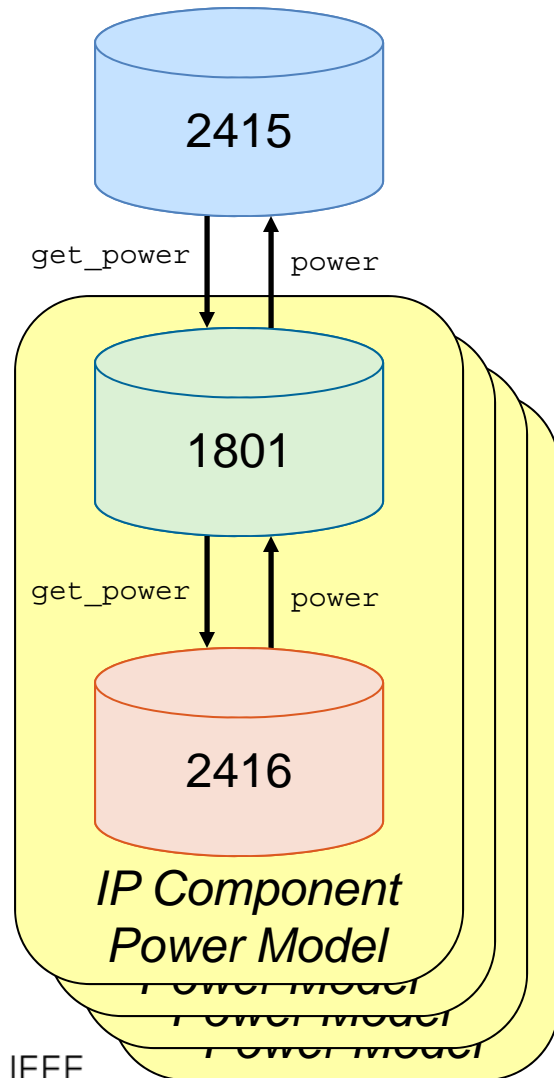


P2415: SW/System Power Model

Vojin Zivojnovic, Chair, IEEE P2415 WG

Power Model Data Flow: 1801-2415-2416

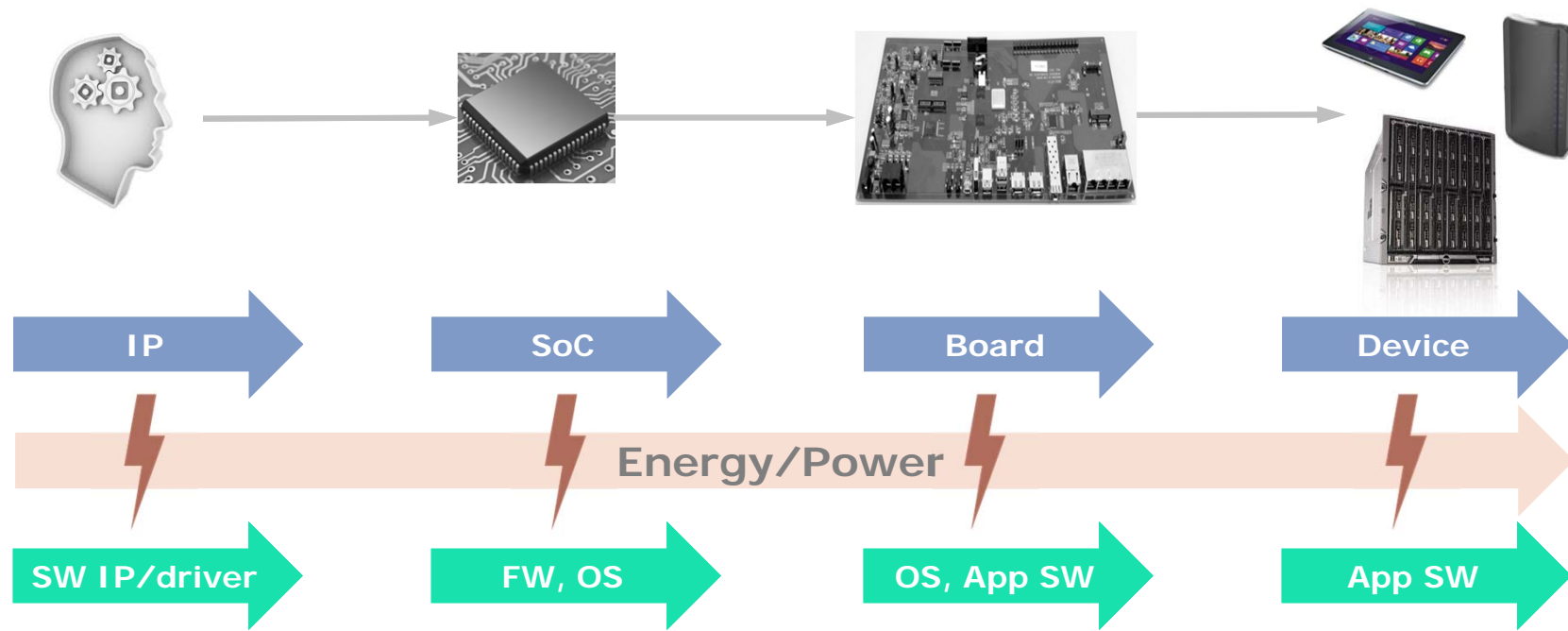


- Unified power abstraction of components and the whole device for FW, OS and apps development
- SW/system-level clocks, voltages, states/transitions, events/control, latencies/power
- Connects the power/energy design flow of HW and SW, IP producers and integrators

- IP Component Power State Model
- Power domains for the component
- Power state definitions per power domain
- Legal transitions between power states
- Power function for each power state

- ▣ IP Component state-based power data
 - Semantics for power/energy views of complex IP
 - Formalized PVT independence
 - Power contributors per (power & functional) mode
 - Energy contributors per mode transition
 - Computationally efficient PVT binding
 - Multi level organization for multiple views

Power Connected HW/SW Flow



IEEE P2415: Unified Hardware Abstraction for Energy Proportional Electronic Systems

P2415: SW/System Power Model

