System Level Power with IEEE1801

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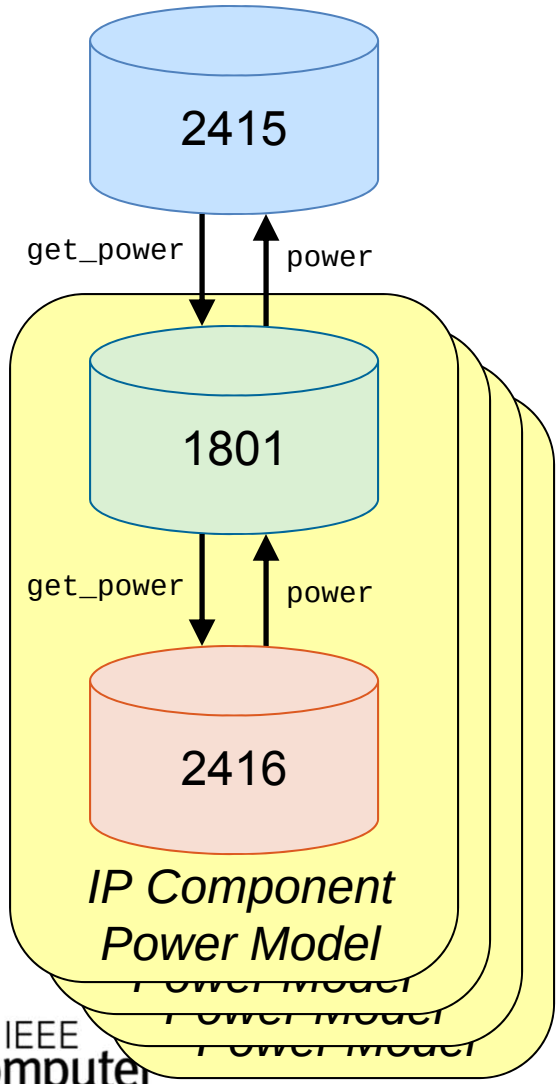
Power Model Data Flow: 1801-2415-2416



- Unified power abstraction of components and the whole device for FW, OS and apps development
- Describes SW/system-level clocks, voltages, states/transitions, events/control, latencies/power
- Connects the power/energy design flow of HW and SW, IP producers and integrators

- IP Component Power State Model
- Power domains for the component
- Power state definitions per power domain
- Legal transitions between power states
- Power function for each power state

- IP Component state-based power data
  - Semantics for power/energy views of complex IP
  - Formalized PVT independence
    - Power contributors per (power & functional) mode
    - Energy contributors per mode transition
  - Computationally efficient PVT binding
  - Multi level organization for multiple views

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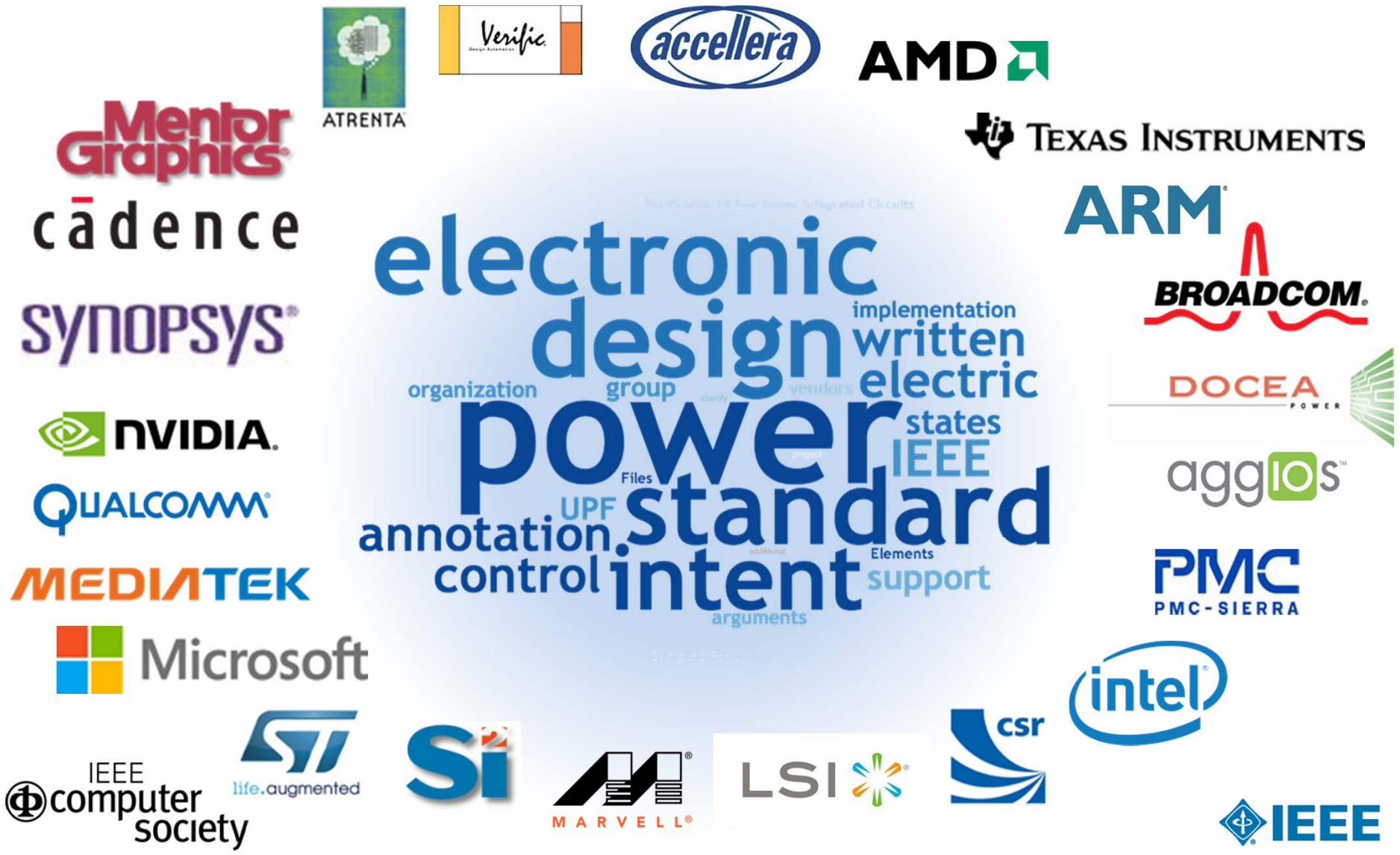
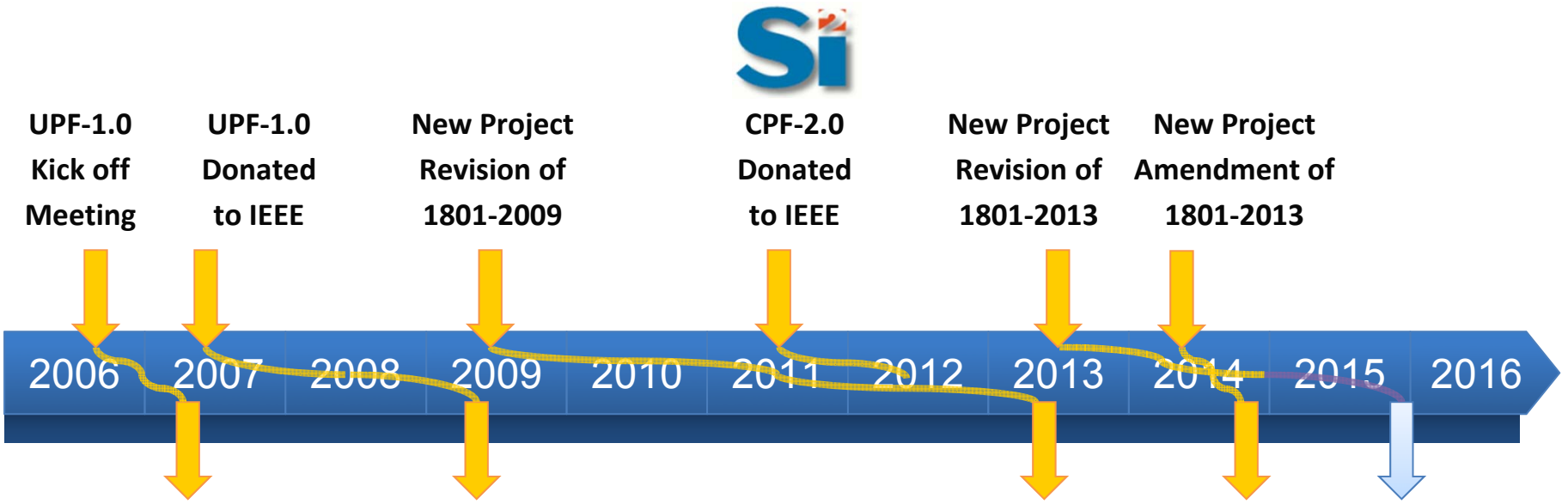
P1801: IEEE-SA Entity Based Work Group



IEEE 1801 Timeline



System Level Power (SLP)

- Challenge: System Level Power depends on perspective:
  - **SW Centric:** abstract, task, transaction/event based
  - **HW Centric:** detailed, component, state/level based

- As an industry we need to bridge this gap:
  - **Top down:** Add detail to the abstract SW centric world of system performance modelling.
  - **Bottom up:** Add abstraction to detailed HW centric world of RTL+UPF implementation

- IEEE 1801: extend UPF as far as appropriate
  - Raise abstraction level of “power intent”
  - Need a better understanding of the system level requirements.

- IEEE 1801: work closely with other standards groups
  - Maximize coherence and interoperability
  - Minimize divergence and duplication

How does 1801 address SLP?

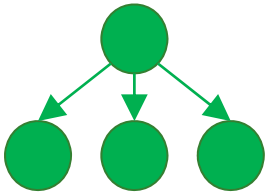
DOES:

- Represent a HW system with component power models
  - begin_power_model, end_power_model
- Define power domains for the component
  - create_power_domain
- Define legal power states for power domains and state transitions
  - add_power_state, add_state_transition
- Identify power function for each power state
  - -state { x -power_expr { … } }

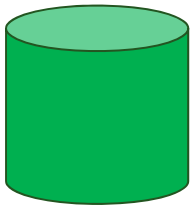
DOES NOT:

- Describe power model stimuli
- Dictate power dissipation algorithms
- Describe characterisation methodology

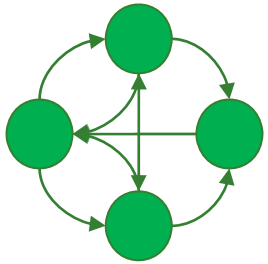
System Level IP Power Model



Enumerated power domains and power states
- All power states of interest within the component
- Power domains defined for major blocks within the IP
- Power states applied to power domains



Interface to IP power characterization data
- Power functions used to calculate power consumption
- Characterization data maintained outside of power model
- Each power state has a defined power function



Definition of all legal power state transitions
- All legal transitions between power states identified
- Activation of power states occurs outside of the model
- Activation only successful for legal power state transitions

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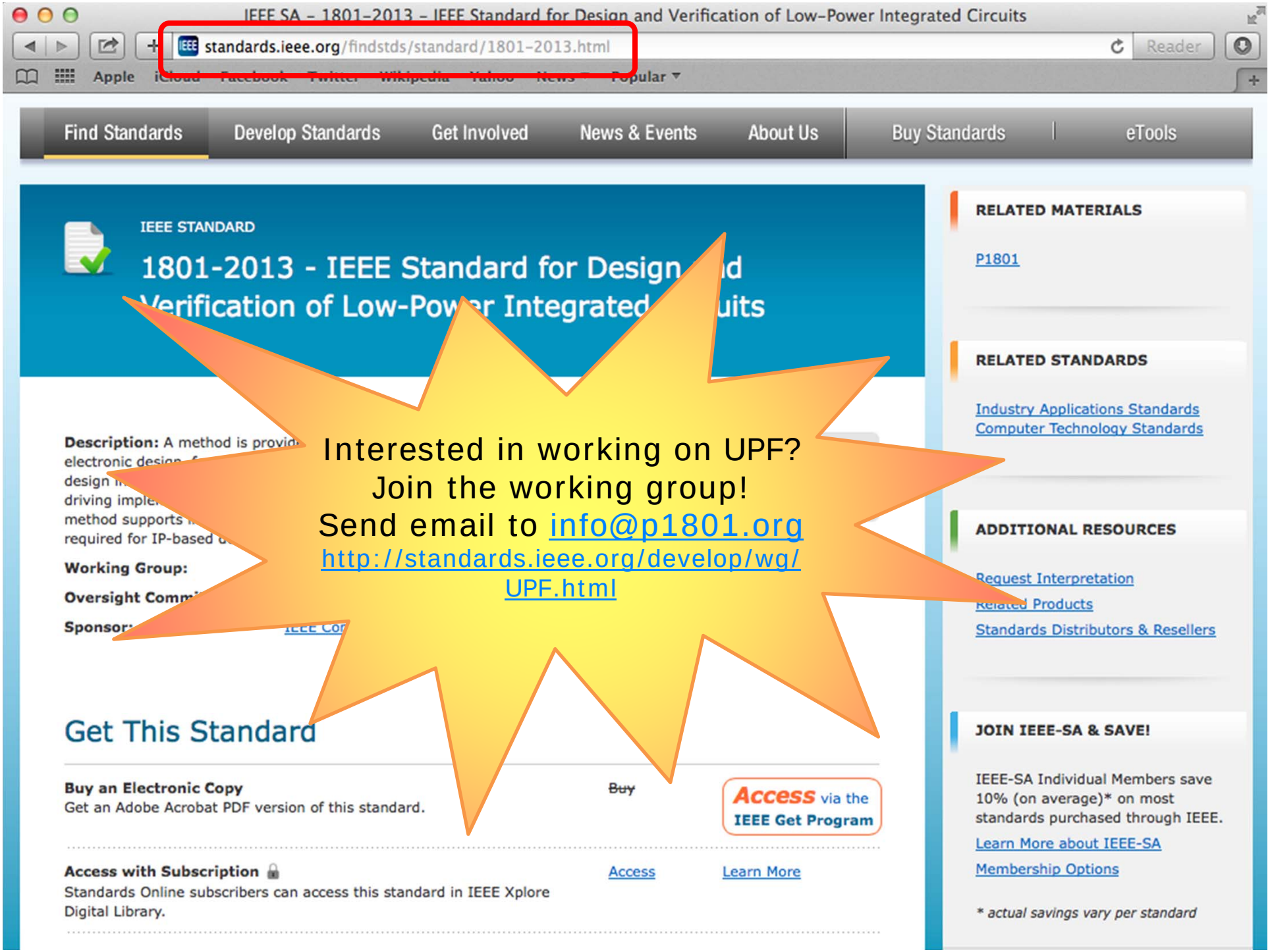
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IEEE 1801-2015 Planned Updates

- **Extend scope of "Power Intent" up towards System Level**
  - **Add power modeling and estimation capabilities**
- Standardised Information Model for query functions and package UPF
- Power States/Transition refinements
- Consider further UPF/CPF methodology convergence
- Enhance and extend Low Power Methodology Annex
- Elaborate on the Successive Refinement methodology
- IEEE1801-2015 to be published late 2015